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Sensing Voltage Transients Using Built-in Voltage Sensor

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Prepared by: Wei Zhang, Zhe Song

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Project Proposal

Introduction

As the feature size of modern integrated circuits is continuously shrinking, the voltage safe margin of state of the art electronic systems is increasingly being tightened. During operation, changes in system activities inevitably cause voltage fluctuations. Due to circuit inductance, current changes in the circuit can cause supply voltage to fluctuate. Other factors like IR drop also contribute to voltage noises in modern ICs. The voltage fluctuation caused by circuit inductance is called voltage transient. If strong enough, voltage transients can cause large swings of supply voltage to bring supply voltage below nominal value (undershoot), which may cause function failures in the system, or above nominal value (overshoot), which may cause permanent hard damage to the system.

Voltage transients often happen when one part or some parts of the circuit suddenly begin to work or stop to work, causing large current changes which further cause voltage changes. As modern processors become increasingly complex and some low power techniques, such as power gating and clock gating, are used, voltage transient is an important factor that deteriorates the voltage safe margins of these modern processors, limiting their nominal voltage far above the minimum to avoid the worst case conditions.

Although voltage transient is a known problem, its characteristics remains unclear. Previous work [1] [3] in this area is limited. Questions like how fast does voltage transient happen, what are its frequency and amplitude are interesting to researchers. To answer these questions, a voltage sensor able to effectively sense voltage noise is needed. To facilitate the study of voltage noise characteristics of modern ICs, in this project we will investigate a new purely digital voltage sensor that can detect voltage transients timely and effectively. Our voltage sensor consists of two key components: a delay line that senses voltage noises and converts them to delays, and a time to digital converter (TDC) that converts the delay to binary digital code. We will build the voltage sensor using the FreePDK 45nm technology and evaluate its resolution, performance and overhead using. We will simulate the voltage sensor and layout it in the project.

The ability to effectively sense voltage noises is very useful in modern ICs. The voltage sensor could be used to detect voltage glitch attacks (an attacker causes voltage glitches in a system and steal secret information from the faulty information) [4], or used to sense voltage fluctuations to indicate the voltage safe margin of a system, such as the IBM critical path monitor [2]. In the project, we will also explore the potential application of the proposed voltage sensors. Some of the areas where the voltage sensor may be used include: security where the voltage sensor can detect any voltage related attacks or the voltage noise could be utilized to produce random numbers, voltage safe margin monitoring, testing purposes where the voltage sensor could be used to test the noise levels within an IC.

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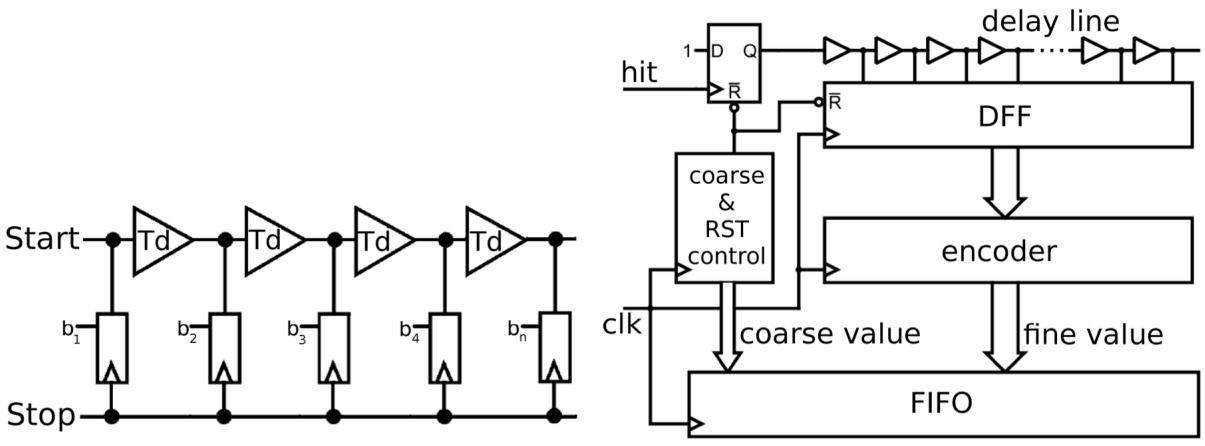
Proposed Project

To effectively sense voltage noises, we propose our voltage sensor design in this project. Our voltage sensor contains two key components: a delay line that senses the changes of the voltage level and converts the changes to delays, and a time to digital converter (TDC) that converts the delay to a binary digital code. In the project, we will investigate the design of the two key components.

The delay line is the component that senses the voltage changes, and the more sensitive the delay line is, the better. The delay line contains a number of delay elements, such as buffers, transmission gate, open latches, or simply a resistor and a capacitor pair. In the project, we will simulate all these delay elements and find out the voltage-delay relationship for each of the components. Based on the voltage-delay profiles arrived at from simulation, we will choose the most appropriate delay element for the delay line.

The TDC is another key component of the voltage sensor. The TDC contains a delay line and a number of flip-flops or latches inserted into the delay line, as shown in Figure 1. Since the TDC is used to convert the delay of the delay line to a binary digital code, we want the delay line in the TDC to be as less sensitive to voltage as possible so that the TDC can work stably even under very worse voltage conditions. Based on the simulation results of the delay elements investigated, the delay element that is most less sensitive to voltage changes will be used as the delay line in the TDC. The sampling components in the TDC could be either the flip-flops, the latches, or the SR latch. The flip-flop needs an extra cycle to get itself reset. The latch can be reset in one half of the clock cycle and sample in the other half of the clock cycle. The SR latch is very sensitive to changes on its input and do not require a clock signal. Each of the components has its advantages and disadvantages, and in the project we will investigate how to make the design decision using simulation method.



(a) Buffer Delay Line schematic (b) Multi-stage Architecture with Delay Line

Figure 1. A time-to-digital converter using delay line.

When the design of the two key elements is finished, we will combine them to form a whole voltage sensor and simulate it. Based on the simulation, we will make corresponding changes to the design. After everything is done, we will layout the voltage sensor and do a post-layout simulation to further verify our design and evaluate it. Finally we will put up with an application where our proposed voltage sensor can be used, and produce a paper if possible.

Simulation Results

Up to now, we have done some simulations of the basic delay elements. The delay elements include buffer, transmission gate, open latch, and RC network. The simulation results are as follows.

Buffer

Buffer is composed of two inverters and it is the basic delay element. In the simulation, we will investigate the relationship between voltage and delay on the buffer. In the simulation, the supply voltage is varied from 1.5V to 0.7V, taking into account the worst voltage conditions. The simulation circuit is shown in Figure 2. The voltage-delay relationship arrived at in the simulation is shown in Figure 3. From the voltage-delay diagram, we can see that the delay of the buffer is positively proportional to the voltage on the buffer. The higher the voltage, the smaller the delay. In addition, the relationship is almost linear. The delay of a buffer in FreePDK 45nm technology under nominal voltage is 19.54ps from the simulation. We will simulate more delay elements and compare them with the buffer.

Voltage (v)	Delay (10^{-12}s)
1.5	17.52
1.4	17.94
1.3	18.38
1.2	18.91
1.1	19.54
1.0	20.14
0.9	21.03
0.8	21.99
0.7	23.12

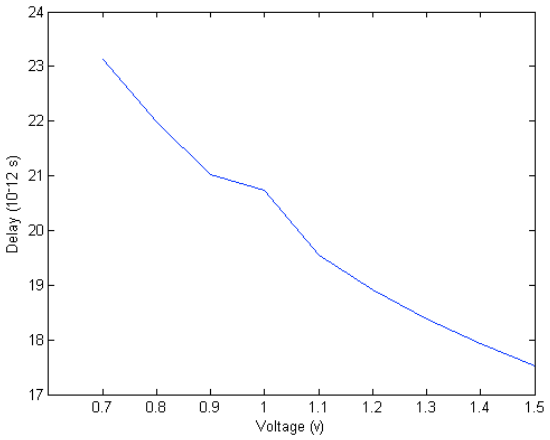


Figure 3. Voltage-delay profile of a buffer (using the FreePDK 45nm technology library).

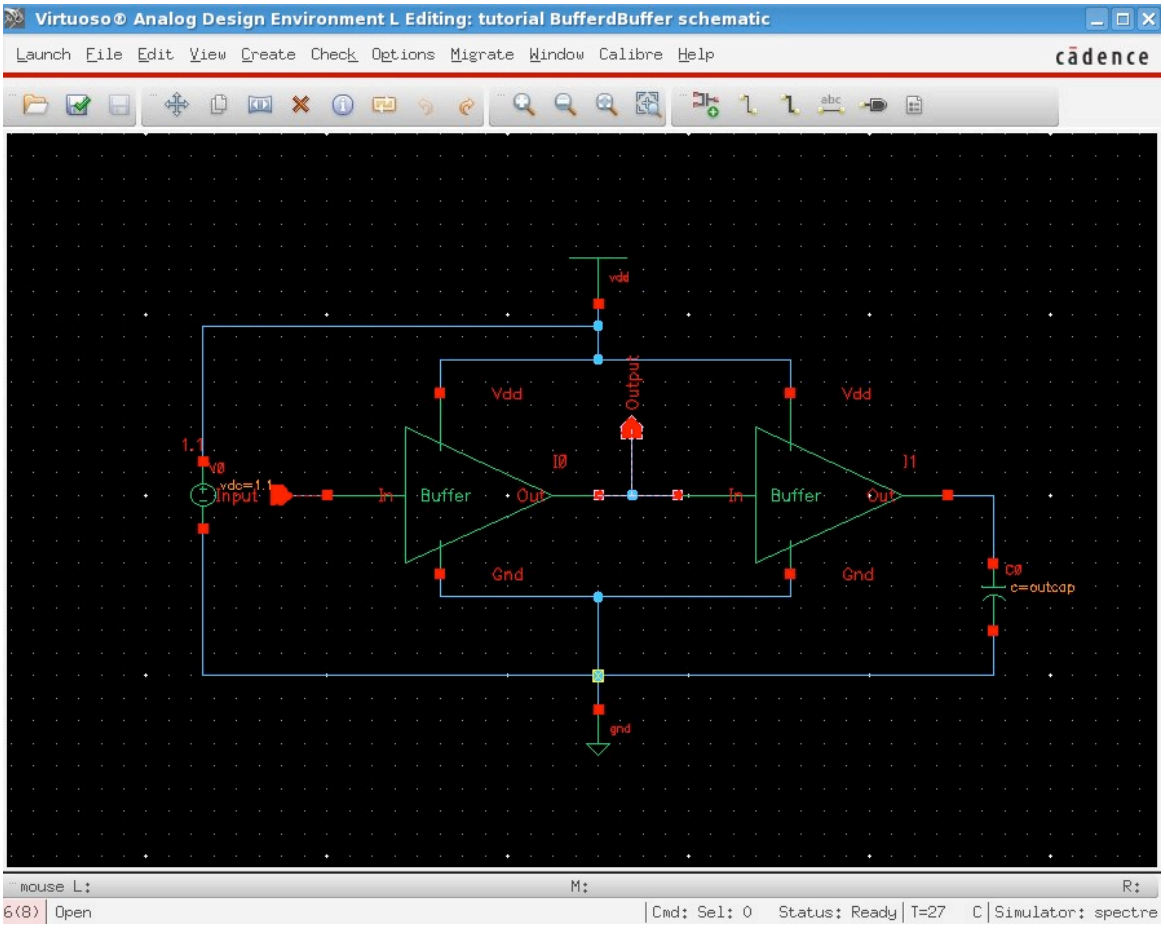


Figure 2. Simulation testbench of a buffer.

Transmission Gate

Transmission gate is another basic delay element that could be used in the delay line. A simulation of the transmission gate's voltage-delay relationship is also performed. The simulation circuits are shown in Figure 4. And the simulation results are shown in Figure 5. The simulation results of the transmission gate is little out of expect and we will look at this later in the project.

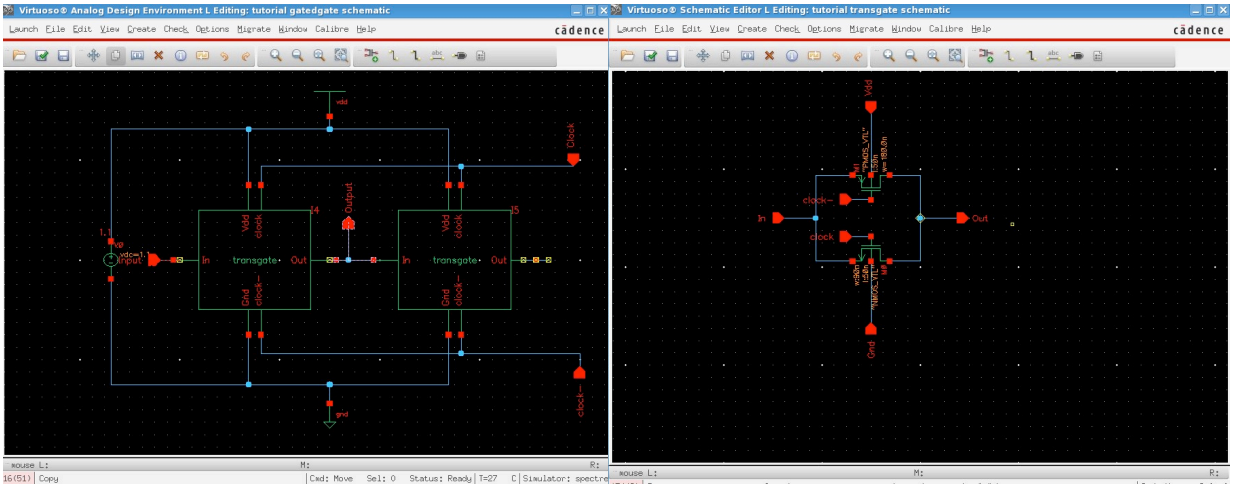


Figure 4. Simulation circuits of a transmission gate.

Voltage (v)	Delay (10^{-12}s)
1.5	398.8
1.4	398.6
1.3	399.0
1.2	398.3
1.1	397.9
1.0	2.616
0.9	3.081
0.8	3.791
0.7	5.096

Figure 5. Simulation results of a transmission gate.

Open Latch

Open latch is another basic delay element that can be used in the delay line. As with buffers, we want to know the voltage-delay relationship for the open latches. The schematic of the latch used in the simulation is shown in Figure 6. The test circuit of the latch is shown in Figure 7. The voltage-delay relationship of an open latch is shown in Table 1. From the simulation results, we can see that generally the higher the voltage the shorter the delay of an open latch is. In addition, the delay of an open latch is much longer than a buffer.

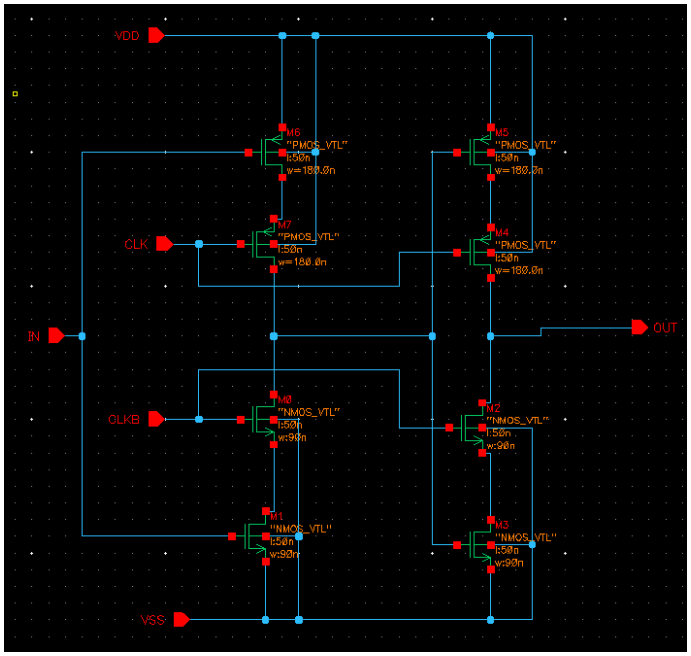


Figure 6. Schematic of the latch.

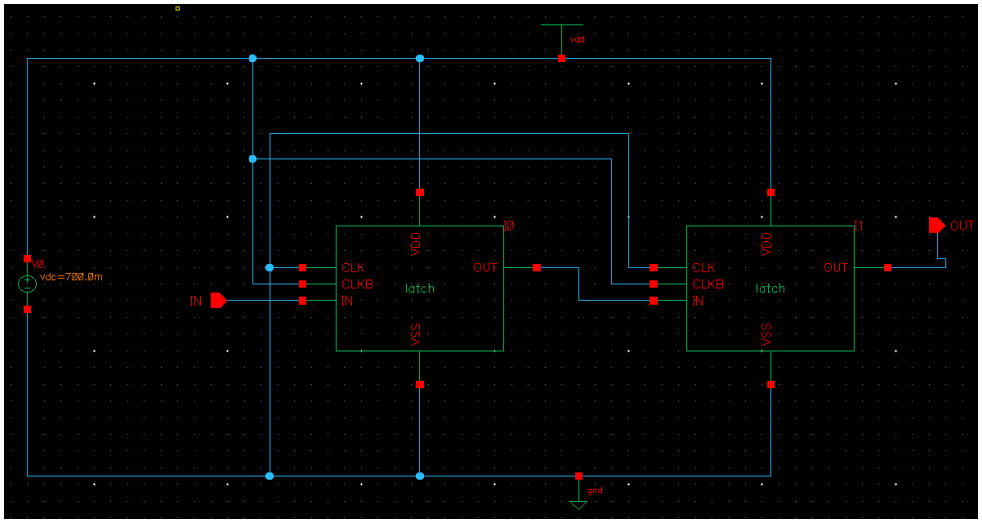


Figure 7. Test circuit used in the simulation of the latch.

Table 1. Voltage-delay relationship of an open latch

voltage (V)	rising time (ps)	falling time (ps)	tp (ps)
1.5	60.6	62.36	61.48
1.4	59	66	62.5
1.3	64.6	61.9	63.25
1.2	67.3	68.31	67.805
1.1	70	68.78	69.39
1	69.7	70.35	70.025
0.9	80.4	77.87	79.135
0.8	78.5	80.05	79.275
0.7	100.1	99.79	99.945

Project Timeline

The project is scheduled to be finished within the course time span. A timeline of the project is shown in Table 2.

Table 2. Timeline of the project.

Tasks	Weeks							
	8	9	10	11	12	13	14	15
Simulate delay elements (buffer, transmission gate, open latch, RC)	✓							
Complete TDC designs and simulate it		✓						
Complete the voltage sensor design and simulate it			✓					
Model voltage transient and evaluate the voltage sensor				✓				
Layout the voltage sensor					✓			
Perform post-layout simulation of the voltage sensor						✓		
Write paper							✓	
Write final report and prepare for presentation								✓

Task Breakdown

The task in the project will be divided between the two members: Zhe Song and Wei Zhang. Zhe will simulate the buffer and transmission gate in the delay line investigation and Wei will simulate the open latch and the RC network. Wei will

design the TDC and Zhe will simulate it. Wei will complete the voltage sensor design and simulate it. Zhe will model the voltage transient and evaluate the voltage sensor. Wei will do the layout of the voltage sensor and Zhe will perform the post-layout simulation of the voltage sensor. And together, Zhe and Wei will write the paper and the final project report.

Conclusion

In this project, we will investigate a voltage sensor that could effectively sense voltage transient noises in modern digital ICs. We will answer those questions mentioned in the above project proposal. Our objective is to finish the sensor design by the end of this course and if possible produce a publishable paper.

References

[1] N. Minas, D. Kinniment, K. Heron, and G. Russell, " A high resolution flash time-to-digital converter taking into account process variability," 13th IEEE International Symposium on Asynchronous Circuits and Systems, pp. 1-10, 2007.

[2] C. Lefurgy et al., "Active management of timing guardband to save energy in POWER7," Pro. Int'l Symp. Microarchitecture (MICRO), pp. 1-11, 2011.

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[4] A.G. Yanci, S. Pickles and T. Arslan, "Characterization of a voltage glitch attack detector for secure devices," Symp. Bio-inspired Learning and Intelligent Systems for Security, 2009.